AP/2815

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: **Herald M. Baldonado**
Serial No.: **10/066,421**
Filed: **01/30/2002**
For: **Method and System of Wire Bonding Using Interposer Pads**

TI No.: **32857**
Art Unit: **2815**
Examiner: **Clark, Sheila**
Conf. No.: **5110**

1# Appeal Brief
9/12/03 DBrown

APPEAL BRIEF TRANSMITTAL FORM

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Elizabeth Austin — August 26, 2003
Date

Dear Sir:

Transmitted herewith in triplicate is an Appellant's Brief in the above-identified application.

Charge any additional fees, or credit overpayment to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. An original and two copies of this sheet are enclosed.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	Conf. No.: 5110
Baldonado, et al.	Docket No.: TI-32857
Serial No.: 10/066,421	Examiner: Clark, Sheila
Filed: 01/30/2002	Art Unit: 2815

For: Method and System of Wire Bonding Using Interposer Pads

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August 26, 2003
Elizabeth Austin

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the Notice of Appeal mailed 06/26/03, Appellant submits this appeal brief in triplicate. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to deposit account number 20-0668 of Texas Instruments Incorporated.

Real Party in Interest

The real party in interest is Texas Instruments Incorporated.

Related Appeals and Interferences

No related appeals or interferences are known to Appellant.

Status of Claims

Claims 1, 2, and 4-21 are pending in this application and are the subject of this appeal. Claims 3 and 22 have been cancelled.

Claims 1, 2, and 4-21 stand rejected under 35 U.S.C. 112, first paragraph.

Claims 1, 2, and 4-21 stand rejected under 35 U.S.C. 102(e) as being anticipated by Schmidt, et al. (U.S. Patent No. 6,232,561).

Status of Amendments

The paper filed by Appellant in response to the final rejection included no amendments other than the cancellation of Claim 22. All other amendments have been entered.

Summary of Invention

In one embodiment, a method and system of wire bonding a semiconductor die 10 to a lead 26 is disclosed (see Figure 2 and accompanying text in the paragraph bridging pages 3 and 4 of the specification). The method includes the steps of: attaching a first end of a first bonding wire 20 to a semiconductor die 10 with a ball bond 12; attaching a second end of the first bonding wire 20 to an interposer pad 21 with a stitch bond; attaching a first end of a second bonding wire 24 to the interposer pad 21 with a ball bond 23; and attaching the second end of the second bonding wire 24 to the lead with a stitch bond 25.

In another embodiment, a semiconductor device is disclosed. (Again, See Figure 2 and the accompanying text in the paragraph bridging pages 3 and 4 of the specification, as well as Figure 6). The device includes a semiconductor die 10 disposed on a substrate; a plurality of interposer pads 21 on the substrate; a plurality of leads 26 on the substrate; a plurality of bonding wires 20, 24 attached to the semiconductor die 10 with ball bonds 12 and to the leads 26 with stitch bonds 25, said wires also attached to the interposer pads 21.

In yet another embodiment, a method of fabricating a semiconductor device is disclosed (See Figure 6 and the text at page 5, lines 6-11 of the specification, in addition to Figure 2 and the text accompanying that figure). The method includes the steps of attaching a semiconductor die 10 to a substrate having a plurality of leads 15, 65 and a plurality of interposer pads 21, 63 arranged around the die; coupling the die 10 to the plurality of interposer pads 21, 63 with a first plurality of bonding wires 20, 61 ball bonded to said die 10 and stitch bonded to said interposer pads 21, 63; and coupling the plurality of interposer pads 21, 63 to the plurality of leads 15, 65 with a second plurality of bonding wires 24, 64 ball bonded to said interposer pads 21, 63 and stitch bonded to said leads 15, 65.

Issues

1. Whether Claims 1, 2, and 4-21 are patentable under 35 U.S.C. 112, first paragraph.

2. Whether Claims 1, 2, and 4-21 are patentable under 35 U.S.C. 102(e) over Schmidt.

Grouping of Claims

Claims 1, 2, and 4-7 stand or fall together. Claims 8-15 stand or fall together. Claims 16-21 stand or fall together. These groups of claims stand or fall independently of one another.

Argument

1. Claims 1, 2, and 4-21 are patentable under 35 U.S.C. 112, first paragraph.

Claims 1, 2, and 4-21 stand rejected under 35 U.S.C. 112, first paragraph. The point of contention in this rejection is whether the original disclosure supports the "attached" features recited in the claims whereby a first end of a

wire is attached by a ball bond and second end by a stitch bond and the first end of a second wire is attached by a ball and the second end by a stitch bond. The Examiner asserts that the only stitch feature is discussed on page 4, line 8 with regard to the bond on lead 26. The Examiner further argues that Figure 4 fails to show the recited stitch features. Appellant respectfully replies as follows: Figure 2 shows one wire (20) attached with a ball bond 12 to die 10. Figure 2 also shows a wire (24) attached with a ball bond 23 to pad 21 and by stitch bond 25 to lead 26. Wire 20 is clearly also attached to pad 21. Since only one ball 23 appears on pad 21, it follows that wire 20 is attached by a stitch bond. One skilled in the art would appreciate that fact in view of the relatively flat profile of a stitch bond that facilitates bonding thereon with a subsequent ball bond. Therefore, Appellant respectfully submits that the "attached" feature is supported in the disclosure.

Claims 1, 2, and 4-21 stand rejected under 35 U.S.C. 112, first paragraph. Specifically, the Examiner asserts that the structure of the interposer substrate is unclear. Appellant submits that the existence of a substrate is clearly implied in the drawings. Moreover, in the "Summary of Invention" section of the specification, the interposer pads are described as being "on an electro-less substrate between the semiconductor die and the lead." Therefore, Appellant submits that the disclosure supports the substrate claim feature. Regarding the term "electroless", Appellant submits that the term taken literally means "insulating." Thus, the die, leads, and interposer pads are formed on an insulating substrate, which is known in the art. The Examiner's assertion in the Advisory Action that the term "electro-less" is well known in the art as a plating process is well taken. However, that is not the only sense in which the word can be used. In this case, the literal meaning of the word is clearly intended and best fits the context in which the word is used, although Appellant appreciates that electroless plating can certainly be used to form the leads and interposer pads of the claimed invention.

The Examiner also asserts that the specification does not support the term "ball grid array." However, the skilled artisan will appreciate that Figures 5 and 6 are top views of an insulating substrate, the underside of which includes pads coupled to leads 15 and 25 in Figure 5 and to leads 65 and 15 in Figure 6. It is known in the art to form solder balls on such pads. As is made clear in the specification, leads 15, 25, and 65 are only representative of the many such leads formed on the substrate. The underside of the substrate includes many such corresponding pads to which solder balls may be attached; hence, the term "ball grid array." Note also the statement on page 5 of the specification that "[t]he disclosed embodiment of the present invention is optimized for use in ball grid array ("BGA") packages, ..." The Examiner's statement on page 5 of the 8/28/02 Office Action that "[p]ads connected to leads are further not conventionally bound to a solder bond substrate underside arrangement" is not understood by Appellant. As indicated in the instant specification, the Microstar ball grid array package from Texas Instruments Incorporated is a package in which leads and pads are connected to solder balls as shown in Figures 1-4. Thus, the Examiner's statement that such an arrangement is not conventional is contrary to Appellant's disclosure.

In view of the electroless or insulating nature of the substrate, the interposer pad is "electrically floating" by virtue of being located on the insulating substrate, a fact which would be appreciated by the skilled artisan.

Regarding the "plurality of interposer pads", Figure 6 shows two interposer pads 21 and 63 which form a plurality.

In view of the above, Appellant submits that the claimed features are fully supported by the disclosure.

2. Claims 1, 2, and 4-21 are patentable under 35 U.S.C. 102(e) over Schmidt.

Claim 1 includes the steps of "attaching a first end of a first bonding wire to a semiconductor die with a ball bond; attaching a second end of the first bonding wire to an interposer pad with a stitch bond; attaching a first end of a

second bonding wire to the interposer pad with a ball bond; and attaching the second end of the second bonding wire to the lead with a stitch bond." Schmidt does not disclose such steps. In fact, Schmidt teaches away from the claimed invention by forming only ball bonds ("welds" in Schmidt's terminology) on his leads 3 and only stitch (or "wedge") bonds on connection surfaces 4 (See Figure 2a of Schmidt). In col. 4, lines 30-37, Schmidt states that this is done to save space on leads 3. Since Schmidt does not disclose all of the features of the claim, Appellant respectfully submits that Claim 1, as amended, as well as Claims 2 and 4-7 which depend therefrom, are patentable over Schmidt.

Claim 8 includes the feature of "a plurality of bonding wires attached to the semiconductor die with ball bonds and to the leads with stitch bonds, said wires attached to said interposer pads." Schmidt does not disclose such a feature. In fact, Schmidt teaches away from forming stitch bonds on leads. Therefore, Appellant submits that Claim 8 and Claims 9-15 which depend therefrom are patentable over Schmidt.

Claim 16 includes the steps of "coupling the die to the plurality of interposer pads with a first plurality of bonding wires ball bonded to said die and stitch bonded to said interposer pads; and coupling the plurality of interposer pads to the plurality of leads with a second plurality of bonding wires ball bonded to said interposer pads and stitch bonded to said leads." Schmidt does not disclose such steps. Therefore, Appellant submits that Claim 16, as well as Claims 17-21 which depend therefrom, are patentable over Schmidt.

Conclusion

In view of the above, Appellant appeals for the reversal of the rejections and allowance of Claims 1, 2, and 4-21.

Respectfully submitted,

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APPENDIX

Claims on Appeal

1. (previously presented) A method and system of wire bonding a semiconductor die to a lead, comprising the steps of:

attaching a first end of a first bonding wire to a semiconductor die with a ball bond;

attaching a second end of the first bonding wire to an interposer pad with a stitch bond;

attaching a first end of a second bonding wire to the interposer pad with a ball bond; and

attaching the second end of the second bonding wire to the lead with a stitch bond.

2. (original) The method and system of wire bonding a semiconductor die to a lead as recited in Claim 1, wherein the first bonding wire and second bonding wire are made of a gold-based material.

3. (cancelled)

4. (original) The method and system of wire bonding a semiconductor die to a lead as recited in Claim 1, wherein the interposer pad is fabricated on an electro-less substrate.

5. (original) The method and system of wire bonding a semiconductor die to a lead as recited in Claim 1, wherein the interposer pad has x-y dimensions of between approximately 58 micrometers to 88 micrometers along an x-axis and 88 micrometers along a y-axis.

6. (original) The method and system of wire bonding a semiconductor die to a lead as recited in Claim 1, for use in ball grid array packages.

7. (original) The method and system of wire bonding a semiconductor die to a lead as recited in Claim 1, for use in MicroStar® ball grid array packages.

8. (previously presented) A semiconductor device, comprising:

a semiconductor die disposed on a substrate;

a plurality of interposer pads on said substrate;

a plurality of leads on the substrate;

a plurality of bonding wires attached to the semiconductor die with ball bonds and to the leads with stitch bonds, said wires attached to said interposer pads.

9. (original) The semiconductor device as recited in Claim 8, wherein the plurality of bonding wires are comprised of a gold-based material.

10. (original) The semiconductor device as recited in Claim 8, wherein the substrate comprises an electro-less substrate.

11. (previously presented) The semiconductor device as recited in Claim 8, wherein each of said bonding wires comprises a bonding wire between the semiconductor die and each interposer pad attached to a bonding pad on the semiconductor die with a ball bond and to said interposer pad with a stitch bond and a bonding wire between the interposer pad and the lead attached to the interposer pad with a ball bond and to each lead with a stitch bond.

12. (original) The semiconductor device as recited in Claim 8, wherein the interposer pads are dimensioned from 58 micrometers to 88 micrometers along an x-axis and from 88 micrometers to 125 micrometers along a y-axis.

13. (original) The semiconductor device as recited in Claim 8, wherein the semiconductor package comprises a ball grid array.

14. (original) The semiconductor device as recited in Claim 8, wherein the semiconductor package comprises a MicroStar® ball grid array package.

15. (original) The semiconductor device as recited in Claim 8, wherein an interposer pad electrically floats on the substrate.

16. (previously presented) A method of fabricating a semiconductor device, comprising:

attaching a semiconductor die to a substrate having a plurality of leads and a plurality of interposer pads arranged around said die;

coupling the die to the plurality of interposer pads with a first plurality of bonding wires ball bonded to said die and stitch bonded to said interposer pads; and

coupling the plurality of interposer pads to the plurality of leads with a second plurality of bonding wires ball bonded to said interposer pads and stitch bonded to said leads.

17. (original) The method of fabricating a semiconductor device as recited in Claim 16, wherein the first and second plurality of bonding wires are comprised of a gold-based material.

18. (original) The method of fabricating a semiconductor device as recited in Claim 16, wherein the plurality of interposer pads electrically float on the semiconductor package.

19. (original) The method of fabricating a semiconductor device as recited in Claim 16, wherein the semiconductor package interposer pads are fabricated on an electro-less substrate.

20. (original) The method of fabricating a semiconductor device as recited in Claim 16, wherein the placement of the interposer pads are operable to reduce wire sweep.

21. (original) The method of fabricating a semiconductor device as recited in Claim 16, wherein the semiconductor package comprises a ball grid array.

22. (cancelled)